IN THE DRAWINGS

Please amend Fig. 2 as indicated on the enclosed copies thereof. Fig. 2 has been amended to illustrate the connection between the clock output from the clock generation part 40 and the phase error estimation part 22 of the phase error detection part 20.

REMARKS

I. Introduction

Applicants would like to thank Examiner Ghulamali for the indication of allowable subject matter recited by claims 2-4. In response to the Office Action dated September 22, 2004, Applicants have amended Fig. 2 so as to illustrate the connection between the clock output from the clock generation part 40 and the phase error estimation part 22 of the phase error detection part 20. No new matter has been added.

Further, Applicants note that the IDS disclosure filed on October 4, 2004 has not yet been considered by the Examiner. Accordingly, it is respectfully requested that the foregoing document be expressly considered during the prosecution of this application, and that the document be made of record therein. If an additional copy of the PTO-1449 form or any of the references is required by the Examiner, the Examiner is respectfully requested to contact the undersigned attorney at 202-756-8372.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claim 1 Under 35 U.S.C. § 103

Claim 1 is rejected under 35 U.S.C. § 103 as being unpatentable over USP No. 5,757,857 to Buchwald in view of USP No. 5,123,030 to Kazawa. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites in-part a clock recovery circuit comprising a phase error detection part including a selection part for selecting, according to the detected variation pattern, whether the estimated phase error is output to the control part.

In accordance with one exemplary embodiment of the present invention, the selection part 24 outputs the estimated phase error if the variation pattern detection signal /3T detected by the pattern detection part 23 is indicated to be at "Hi" level. On the other hand, zero is selected if the variation pattern detection signal /3T detected by the pattern detection part 23 is indicated to be at "Lo" level. Accordingly, the selection part 24 selects and outputs a phase error detection signal to the control part 30 (see, e.g., page 8, lines 13-20 of the specification). As a result, the present invention advantageously provides protection against unlocking of the PLL by preventing a phase error "misdetect" in the clock recovery circuit.

Turning to the cited prior art, neither Buchwald nor Kazawa disclose or suggest selecting, according to the detected variation pattern, whether the **estimated phase error** is output to the control part. In direct contrast, Kazawa discloses that the output clock pulses 102 delivered from the PLL 3 are converted into the baud clock pulses of 4 MHz 103 by the frequency divider 4, while the clock pulses of the opposite phase 108 are generated by the NOT gate 56, such that the switch 57 of the distinguisher 5 applies a **selected one of the above clock pulses 103 and 108** to the discriminator 7 (see, col. 8, lines 50-59). As such, contrary to the conclusion set forth in the pending rejection, Kazawa merely discloses outputting a clock pulse, rather than a signal indicating the phase error, to the discriminator 7. For at least these reasons, it is respectfully submitted that Kazawa teaches away from the claimed invention. On the other, Buchwald, as acknowledged by the Examiner, does not disclose or suggest a selection part, and therefore also does not cure this defect of Kazawa.

Accordingly, as each and every limitation must be either disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (see, **M.P.E.P. § 2143.03**), and

Buchwald and Kazawa, taken alone or in combination, fail to do so, it is respectfully submitted that claim 1 is patentable over the prior art.

III. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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